


System simulations of a 1.5 V SiGe 81–86 GHz E-band transmitter

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Abstract This paper presents simulation results for a sliding-IF SiGe E-band transmitter circuit for the 81–86 GHz E-band. The circuit was designed in a SiGe process with $f_T = 200$ GHz and uses a supply of 1.5 V. The low supply voltage eliminates the need for a dedicated transmitter voltage regulator. The carrier generation is based on a 28 GHz quadrature voltage oscillator (QVCO). Upconversion to 84 GHz is performed by first mixing with the QVCO signals, converting the signal from baseband to 28 GHz, and then mixing it with the 56 GHz QVCO second harmonic, present at the emitter nodes of the QVCO core devices. The second mixer is connected to a three-stage power amplifier utilizing capacitive cross-coupling to increase the gain, providing a saturated output power of +14 dBm with a 1 dB output compression point of +11 dBm. E-band radio links using higher order modulation, e.g. 64 QAM, are sensitive to I/Q phase errors. The presented design is based on a 28 GHz QVCO, the lower frequency reducing the phase error due to mismatch in active and passive devices. The I/Q mismatch can be further reduced by adjusting varactors connected to each QVCO output. The analog performance of the transmitter is based on ADS Momentum models of all inductors and transformers, and layout parasitic extracted views of the active parts. For the simulations with a 16 QAM modulated baseband input signal, however, the Momentum models were replaced with lumped equivalent models to ease

simulator convergence. Constellation diagrams and error vector magnitude (EVM) were calculated in MATLAB using data from transient simulations. The EVM dependency on QVCO phase noise, I/Q imbalance and PA compression has been analyzed. For an average output power of 7.5 dBm, the design achieves 7.2% EVM for a 16 QAM signal with 1 GHz bandwidth. The current consumption of the transmitter, including the PA, equals 131 mA from a 1.5 V supply.

Keywords E-band · MM-wave · EVM · Transmitter · Power amplifier · 16 QAM · SiGe

1 Introduction

High capacity Gb/s wireless point-to-point communication links can be implemented in the E-band at 71–76 and 81–86 GHz. Optical fiber has previously been preferred for the backhaul networks [1, 2]. However, it is not always possible to deploy an optical fiber due to regulations, installation time and cost [1, 2]. In the upcoming 5G heterogeneous networks the number of base stations will increase, making a wireless backhaul more favorable. In Europe, the 5 GHz spectrum of each sub-band is divided into 250 MHz channels [2, 3] which can be merged if higher data capacity is required. In the United States the bands are instead divided into 1.25 GHz channels [4]. A typical E-band transceiver product consists of several MM-wave ASICs plus external power amplifiers (PAs). In [2, 5] a SiGe E-band transceiver product is presented, demonstrating a 3.18 Gbps radio link using 256-level quadrature amplitude modulation (QAM) [6] in a 500 MHz RF channel bandwidth, with 8 dBm output power at the antenna. The architecture consists of separate receiver and

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transmitter ASICs, an external phase locked loop (PLL) together with an external power amplifier (PA) and low noise amplifier (LNA) in GaAs-technology. In industry, there has so far been less focus on integration level of E-band transceivers. Compared to chipsets for cellular communication, the integration level for E-band transceivers is therefore still low. As the volumes of wireless links will increase with the deployment of the upcoming 5G networks, integration level will be a key driver for product cost reduction. To address this, in this paper, a 1.5 V E-band transmitter for the 81–86 GHz E-band is presented. The transmitter is fully integrated, i.e. it consists of upconversion mixers together with an integrated PA that share a common supply. The upconversion is based on an on-chip 28 GHz QVCO [7–9], which creates four LO phases for an I/Q upconversion mixer for the baseband signal. In a second mixing stage, the 56 GHz second harmonic, present at the emitter nodes of the QVCO core devices, upconverts the 28 GHz signal to 84 GHz [7–10]. Using a single supply voltage of only 1.5 V for the entire transmitter eliminates the need of a dedicated voltage regulator, since, the supply can then be shared between the transmitter and the digital control circuits. The low supply three-stage PA uses capacitive cross-coupling [11–15] to increase the power gain and isolation of each stage. Early E-band transmitters used simple modulation schemes such as binary phase-shift keying (BPSK) or on–off keying (OOK) [1]. These modulation schemes do not require a high linearity transmitter but are on the other hand less spectral efficient [16]. In E-band systems of today, to support spectral efficient transmission with high data rates, M-ary QAM is used. For low bit-error (BER), data links using QAM modulation put more stringent requirements on transmitter nonidealities, resulting in tight error-vector-magnitude (EVM) specifications [17–22]. In this paper, the effects on simulated EVM, for a 2 GHz 16 QAM signal, of local oscillator (LO) phase noise, I/Q imbalance, and PA compression are therefore investigated. Transient simulations were performed using parasitic extracted views of the circuit parts and lumped model equivalents of the inductors and transformers. The EVM was calculated by importing the demodulated data into MATLAB. For each modulation scheme, there is a known relationship between EVM and bit-error-rate (BER) [22]. Using the EVM as a metric to evaluate the performance is advantageous, since more time consuming BER calculations can then be avoided at an early stage of the design phase [22]. The transmitter was designed in a 0.18 μm SiGe HBT process, with four Cu metal layers with a top layer thickness of 2.8 μm , and with an f_T of 200 GHz. The process does not have any MOS devices. In this paper the presented transmitter and the EVM simulation setup are first briefly discussed. In Sect. 2, the transmitter architecture is described together with a

comparison to other transmitter topologies. The design of the different circuit parts is then discussed in Sect. 3. In Sect. 4, the design and layout of the inductors and transformers are presented, together with the layout of the complete transmitter, including the power amplifier. The simulation results for a non-modulated baseband signals are provided in Sect. 5. In Sect. 6, the EVM as a metric to analyze transmitter imperfections is discussed together with the simulation setup. A flow chart for the developed MATLAB program for EVM calculation is described and the simulation results are presented. The conclusions are given in Sect. 7.

2 Transmitter architecture

There are several possible architectures for creating an E-band TX carrier. Direct conversion architectures [23–25] are often used, however, with different implementations of the generation of the LO frequency. In [23], digital correction is implemented. In [24], a direct conversion E-band transmitter, using an external LO, was simulated and measured. Polyphase filters were used to create quadrature LO signals. Since a direct conversion architecture is susceptible to process mismatch, the work is focused on tuning methods to suppress LO feed-through and I/Q imbalance, using I/Q phase calibration to improve the EVM. The 84 GHz TX carrier can also be generated using injection lock techniques. In [26], a 90 GHz carrier was generated from a 30 GHz VCO using either injection locked or harmonic-based LO tripler circuits. An 84 GHz quadrature injection locked oscillator (QILO) can be injection locked by a 28 GHz VCO [27]. A 60 GHz PLL based on an N-push 20 GHz VCO was presented in [28]. A 3-push VCO consists of three coupled VCOs with a phase difference of 120° between them. By combining the VCO outputs, the fundamental tone as well as the second harmonic can be cancelled, leaving only the third harmonic at 60 GHz. Quadrature LO signals can be created with either a polyphase filter (PPF) or hybrid coupler (HC) [28]. At 84 GHz, the I/Q mismatch of both PPFs and HCs will, however, be significant. In [29, 30] a sliding-IF E-band transceiver circuit was therefore presented, covering both the 71–76 GHz and the 81–86 GHz band, providing 15.2 dBm of output power in the upper band. The transmitter was based on a 19 GHz PLL. The PLL output is supplied to an I/Q divide-by-two block that generates the LO signal for an I/Q up conversion mixer for the baseband signal. Upconversion to 85.5 GHz is then performed by mixing with the quadrupled 19 GHz signal from the PLL. A driver amplifier, also providing the necessary image rejection before the PA, consumes 42 mA. In [30], measurement results for the design in [29] were presented for the lower

E-band at 71–76 GHz, achieving a P_{sat} of 20.5 dBm. The complete transmitter, including the PLL, consumes 200 mA from a 2.7 V supply, plus 500 mA from a 2 V supply for the PA at P_{sat} .

In the presented sliding-IF transmitter architecture, given in Fig. 1, a 28 GHz QVCO [7–9] is used to generate the 84 GHz TX carrier in two steps [10]. A direct conversion architecture, with a QVCO operating at the 84 GHz carrier frequency, is not preferred due to stringent requirements on I/Q phase error for higher order QAM modulation [17–20]. The effect of device mismatch is worse for a higher frequency QVCO and I/Q mixer. Instead, in this work, a 28 GHz I/Q mixer first up-converts the baseband signal. The 84 GHz TX signal is then generated by mixing with the 56 GHz differential second harmonic inherently present at the emitters of the cross coupled QVCO transistors [7–10], thereby eliminating the need for current-consuming frequency doubler circuit blocks.

The conversion gain of the active mixers depends on the amplitude of the signal driving the bases of the current commuting devices. Below a certain signal level, there is a significant reduction of conversion gain. LO-buffers are therefore placed before both the 28 and 56 GHz mixers to secure a sufficient LO level. In [8, 9] the 28 GHz QVCO was locked to an external 1.75 GHz reference signal in a PLL. A buffer was then used to isolate the QVCO from the PLL divider. For symmetry reasons, two buffers are therefore connected to the I- and Q-output, respectively, of the QVCO. In [8, 9], beam steering was also implemented by DC current injection into the load of a Gilbert type phase detector [31] of the PLL [10].

3 Transmitter circuit blocks

3.1 QVCO

Simulation and measurement results for the 28 GHz QVCO, see Fig. 2, both standalone [7, 8] and in a PLL [9]

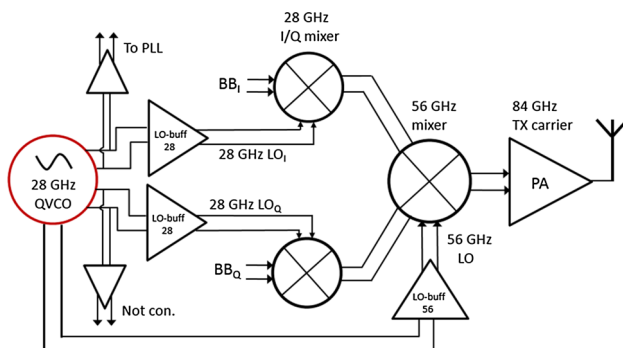


Fig. 1 Architecture for an 84 GHz transmitter from a 28 GHz QVCO

have been previously presented. To minimize the I/Q phase error, phase tuning [7, 8] has been implemented. The QVCO in this paper consists of two cores, Fig. 2(a), connected together as in Fig. 2(b). The main and injection stages were designed with bias currents of 5.8 mA and 1.0 mA, respectively, i.e. the QVCO total bias current equals 13.6 mA. To improve the layout symmetry there are two main varactors, implemented as reversed biased pn-junctions using a control voltage V_{ctrl} . The QVCO inductors, with a layout shown in Fig. 4, are represented by inductors L_{VCO} in Fig. 2(a). The inductors were simulated and modeled using ADS Momentum. Each QVCO core in Fig. 2(a) contains two phase error tuning blocks biased with control voltages V_{tune_p} and V_{tune_n} . With two QVCO cores there are four tuning blocks in total, biased with control voltages from 0 to 7.7 V. The I/Q phase error can be minimized by changing these control voltages [7, 8], providing a simulated phase tuning range of 14.5° [7].

In this paper, a transformer, as indicated in Fig. 3, is added at the tail of the main stage to extract the 56 GHz second harmonic. The transformer has two center taps. The center tap on the primary side is connected to the collector of the biasing device [10], while the center tap on the secondary side is used for biasing of the 56 GHz LO buffer, shown in Fig. 4(b). The QVCO in Fig. 3 is biased with 8.1 mA and 1.0 mA in each main and injection stage, respectively. The main current was increased in order to increase the oscillator performance.

In the simulations of large signal linearity and EVM, the QVCO with 56 GHz output schematic was replaced with a Verilog-A model based on the oscillator in the standard Cadence module library rLib. Using control parameters for the Verilog-A module, the phase noise can be shaped for a slope of either 20 dB/decade or 30 dB/decade. The four phases of the 28 GHz QVCO are created using time delays. The 56 GHz output is generated from a frequency multiplier. By replacing the transistor level QVCO with a Verilog-A model, it is possible to simulate the complete transmitter using the periodic steady-state analysis (PSS) in Cadence SpectreRF. Due to simulator convergence difficulties, this is not possible using PSS oscillator mode for the design in Fig. 3. The EVM calculations are based on a transient analysis, which would have been too time consuming if a device-level representation of the QVCO had been used.

3.2 LO buffers

Two 28 GHz buffers, with a topology outlined in Fig. 4(a), are placed at the I and Q QVCO outputs.

The 28 GHz buffer was biased with a tail current of 3.4 mA and loaded with resistors R_2 of 60 Ω . This results in a differential output signal of 170 mV_p at the base

Fig. 2 QVCO core schematic and architecture [7]. **a** QVCO core schematic. **b** QVCO architecture

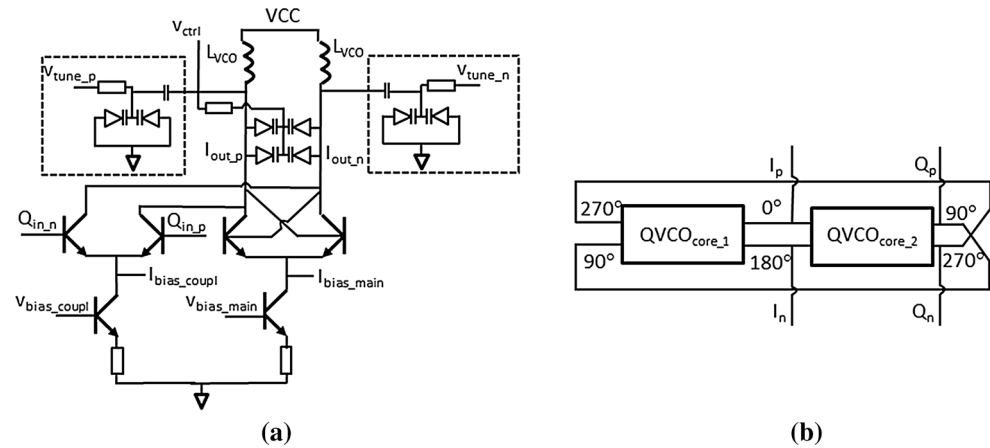


Fig. 3 QVCO architecture with 56 GHz output transformer excluding I/Q phase error tuning

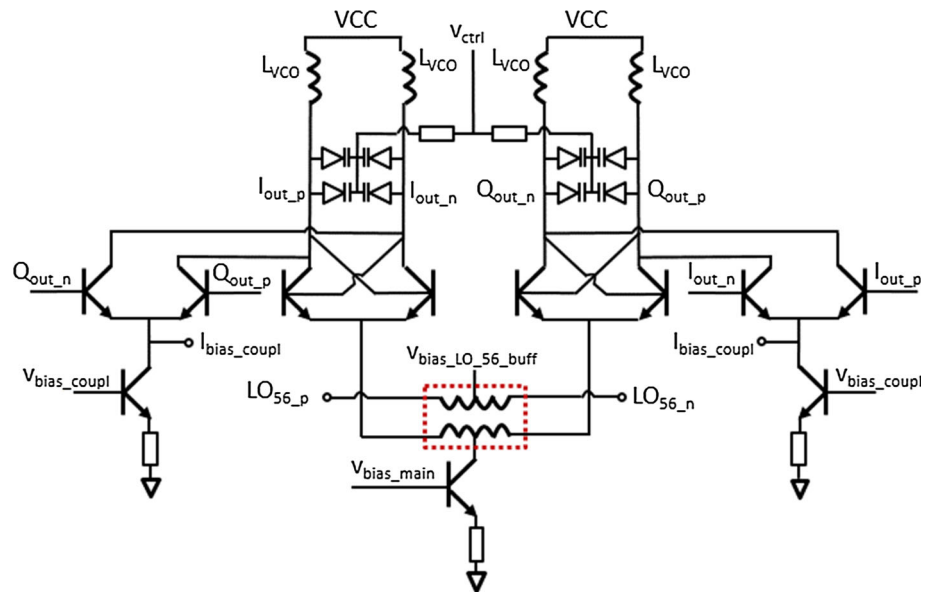
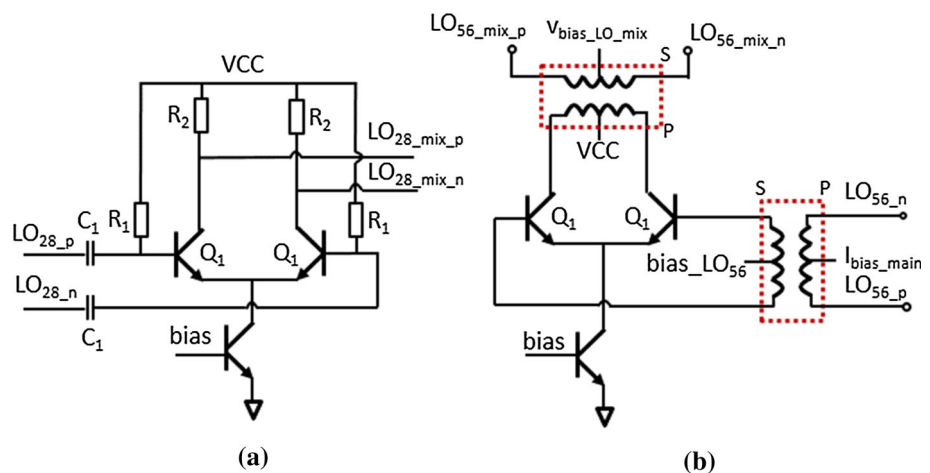


Fig. 4 28 GHz LO buffer (a) and 56 GHz LO buffer (b)



terminals of the 28 GHz mixer. Since the buffer is operating at only 28 GHz, the output voltage amplitude is large enough without having to implement an inductor at the

output to resonate with the capacitive parasitics. For the 56 GHz LO buffer, see Fig. 4(b), the transformer primary side input nodes, LO_{56_p} and LO_{56_n} , are connected to the

emitters of the main QVCO devices. The main devices of the QVCO are biased through the primary side center tap connection I_{bias_main} , while the base terminals of the 56 GHz buffer are biased through the secondary side center tap connection $bias_LO_{56}$. The 56 GHz buffer output transformer is connected to the bases of the switching devices of the 56 GHz mixer. The buffer is biased with 3.9 mA, giving a differential voltage swing of 150 mV_p at the base terminals of the 56 GHz mixer.

3.3 Mixers

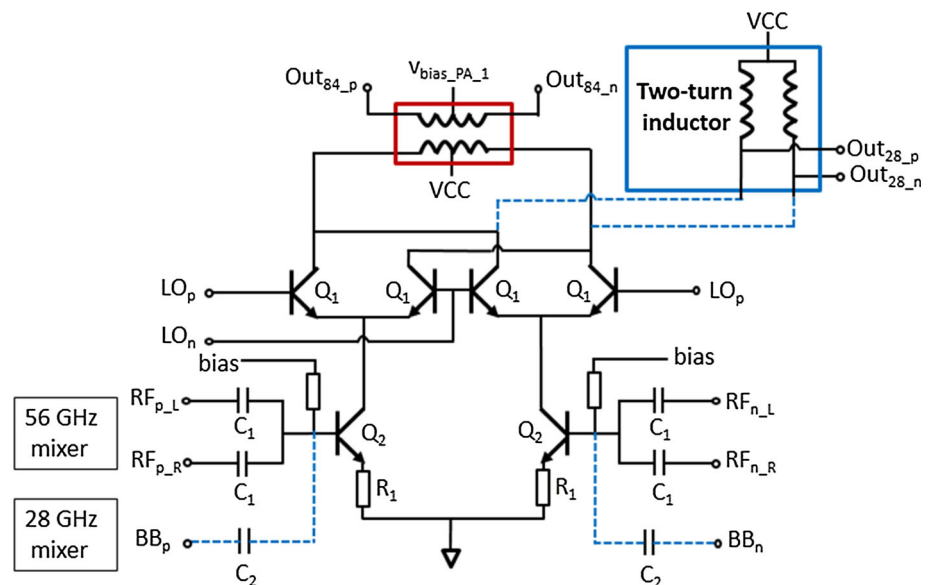
The core topology of the 28 GHz and 56 GHz active double balanced active mixer is given in Fig. 5. The mixer topologies are identical, except for the input signal connection to the transconductance stage and the inductor/transformer at the output. The 28 GHz mixer upconverts the baseband signal with the signal from the 28 GHz LO buffers in Fig. 4(a). The output nodes, Out_{28_p} and Out_{28_n} of the load inductor are connected to the transconductance stage input of the 56 GHz mixer. Two turns are used to reduce the die area of the load inductor. The inductance is designed to resonate at 28 GHz with the output capacitance of the 28 GHz mixer plus the input capacitance of the 56 GHz mixer. The baseband signals, BB_p and BB_n , are AC-coupled to the 28 GHz mixer transconductance stage with capacitors C_2 . Each transconductance device is biased with 4.7 mA and degenerated with a resistor R_1 equal to 5 Ω to increase the mixer linearity.

The 56 GHz double balanced active mixer has output nodes, Out_{84_p} and Out_{84_n} , connected to the input of the PA. The transconductance devices Q_2 are biased with 12 mA each. The current commuting devices Q_1 are

scaled so that the maximum allowed current density, i.e. 6.5 mA/ μm^2 , is not exceeded when all devices Q_1 are turned on simultaneously. For maximum power transfer to the PA, the mixer output transformer, with a layout shown in Fig. 8, is designed to be in resonance with the parasitic output capacitance of mixer devices Q_1 plus the input capacitance of the PA. This sets a bias current constraint of the 56 GHz mixer, since a larger bias current, resulting in an increased mixer conversion gain and output compression point (OCP_{1dB}), requires larger devices Q_1 . Larger devices, however, have a higher output capacitance, which requires the inductance of the mixer output transformer to be reduced to maintain resonance. However, for the transformer to have a low insertion loss, there is a lower limit for its inductance.

The selected bias current of 12 mA optimizes the combined performance of the mixer and output transformer. The devices Q_1 are switched with a differential LO-signal with an amplitude of 200 mV_p. For layout reasons, summation of the signals from the I- and Q 28 GHz mixer outputs is made after the AC-coupling capacitors C_1 , equal to 800 fF each. The OCP_{1dB} of the 56 GHz mixer must be large enough so that it does not limit the compression point of the transmitter. To maintain the compression point across the 81–86 GHz band, the input matching of the PA is designed to be wideband with $S_{11} < 10$ dB between 75 and 95 GHz. A critical design parameter is the connection distance from the secondary side of the 56 GHz LO buffer transformer to the bases of the switching pair in the 56 GHz mixer. In comparison with the inductance of the transformer, the series trace adds significant inductance. The series inductance was therefore minimized by using the design kit maximum allowed trace width of 10 μm . To increase the mixer linearity, the

Fig. 5 28 and 56 GHz mixer architecture



transconductance devices, Q_2 , are degenerated with resistors R_1 equal to $10\ \Omega$.

3.4 Power amplifier

The power amplifier architecture is shown in Fig. 6. It is a three stage differential design with interstage matching in between, sharing the transmitter supply voltage of 1.5 V. The fewer the stages, the higher the power added efficiency, (PAE) [11–15, 32, 33] of the PA. For the presented transmitter, the minimum number of stages is limited by the output compression point of the 56 GHz mixer. With a two stage PA [14, 15], the maximum output voltage swing from the 56 GHz mixer is not enough to drive the PA into compression ($\text{OCP}_{\text{dB}} = -4.0\ \text{dBm}$), and therefore an additional stage is required as a preamplifier.

In order to minimize the reduction in PAE, the bias current of the different stages is increased from input to output. In conventional bipolar PA designs, a cascode stage [32, 33] is used to increase the gain and provide isolation between the different stages. In this paper, however, due to the limited supply voltage of 1.5 V, a cascode architecture could not be used. Instead, the high frequency gain, as well as the isolation, was increased using a common emitter stage with capacitive cross-coupling [11–15].

The topology of the first and second stage, depicted in Fig. 7(a), are identical except for device sizes and bias currents. The effective emitter area of the devices in each stage is given in Fig. 7(b). The third stage, differs slightly, as it has capacitors in series with the input terminals, as part of an impedance up-transformation network, see Fig. 8. The transistors have a parasitic base–collector capacitance, C_{bc} , that reduces the power gain as well as the isolation between the input and output nodes of the common emitter stages [11–15]. The capacitive cross coupling technique reduces the effect of the base–collector capacitance. It has been implemented with diode connected devices Q_2 , with a capacitance $C_{bc\text{-}diode}$ [12, 14, 15]. Capacitive cross coupling could also be implemented in two other ways, either with fixed metal–insulator–metal (MIM) capacitors or with controllable capacitors, implemented as diode junctions in series with MIM capacitors [14]. Due to process spread, the topology with fixed MIM capacitors was not chosen. With diode connected devices

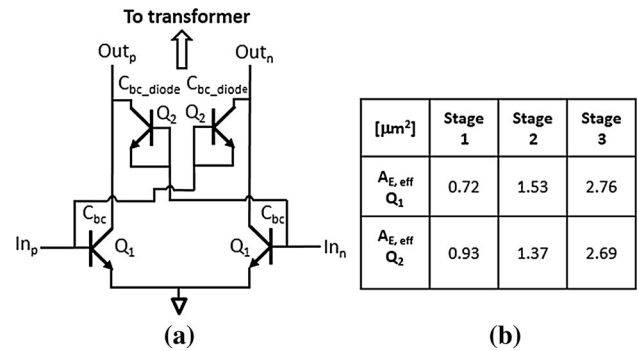


Fig. 7 Architecture of the PA stage 1 and 2 (a) and device sizes (b)

there are benefits both regarding process spread, and large signal behavior [12, 15]. All devices are of the same type, which reduces the effects of mismatch.

Since for high output power, the voltage swing across the base–collector junctions will be high enough to cause significant modulation of the capacitance, using cross-coupled diode connected devices is highly beneficial, since the effective capacitance modulation will then be significantly reduced [12]. The bias currents of the three stages were set to 4.5 mA, 9.8 mA and 16 mA, respectively. Using capacitive cross coupling, there is a clear tradeoff between gain, stability and input matching bandwidth. Using too large a value of the cross coupling capacitance results in a large increase in maximum available gain, G_{max} , but on the other hand, the stability factor, k [11, 14, 15, 34] is then less than unity, i.e. the design is not unconditionally stable [11, 34]. At the same time, the input impedance increases, and the input matching bandwidth decreases, making the design sensitive to process spread. For a robust design, there is thus a limit on how much the gain can be increased in each stage while maintaining a sufficient bandwidth.

Single turn transformers with center tap biasing on both primary and secondary side [35] are used as interstage matching between all stages of the PA. Compared to using inductors, the transformer structures are more convenient for connecting two stages together, since in layout, input and output terminals are opposite to each other. To increase power transfer between two stages, the transformer is designed to be in resonance with the output capacitance of the first stage and the input capacitance of the second stage.

Fig. 6 Three-stage power amplifier architecture

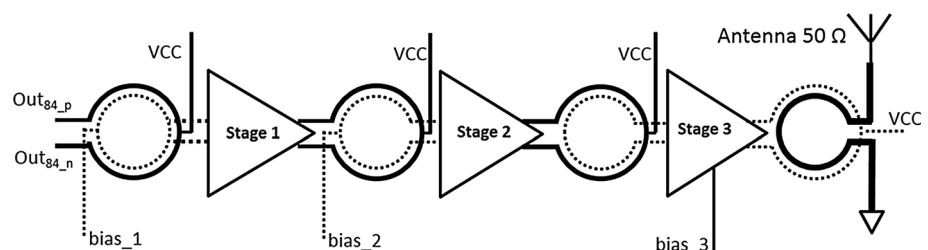
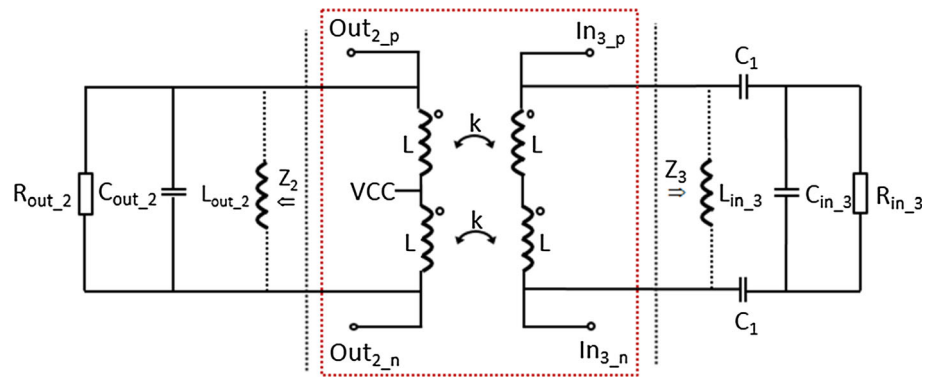


Fig. 8 Transformer interstage matching between PA stage two and three



Between stage two and three, a combination of transformer resonance and impedance transformation is utilized, as shown in Fig. 8 [15]. The output impedance of stage two is represented by resistor R_{out_2} and capacitor C_{out_2} .

The input impedance of stage three is up transformed with a combination of series capacitors C_1 equal to 110 fF and a shunt inductance L_{in_3} , giving a real up transformed input impedance, Z_3 , of 200 Ω , i.e. an impedance transformation of 3.6 times [15]. Without up transformation, the second stage would be loaded by a low impedance, effectively reducing the power gain. A transformer is used to connect stage two and three together, replacing the output resonance inductance of stage two, L_{out_2} , and the input matching inductance of stage three, L_{in_3} .

4 Inductor/transformer design and transmitter layout

4.1 Electromagnetic simulation

In a MM-wave transmitter design, accurate models of inductors and transformers are needed. In this paper, the ADS Momentum 2.5D electromagnetic simulator has therefore been used to extract S-parameter models for the inductive parts. Since the gain of the active devices in the used technology is limited at 84 GHz, almost all interface nodes between the circuit parts are in resonance to maximize the power transfer. Any modeling error can therefore result in significant loss in signal transfer. For the presented transmitter, intended for higher order QAM modulation, also the matching between different inductive elements is important, since any imbalance can result in impairments of the transmitted signal [17–20]. Even small imbalances in capacitive parasitics, in the range of a few femtofarads, can result in I/Q phase errors that cause significant degradation in the BER [7, 8] of the radio link. It is therefore important to design a well-balanced layout of both the QVCO core and its routing to minimize the error. In case of a residual phase error, this can be

minimized using the I/Q phase tuning of the QVCO in Fig. 2(a) [7, 8]. The octagonal inductors of the QVCO together with the routing to the 28 GHz LO buffers, as well as the routing to the PLL divider buffers [8, 9] are shown in Fig. 9. A similar structure has been used in both a PLL and a QVCO plus I/Q phase error detector circuit [7–9]. In the PLL design [8, 9], only the Div_{Q_p} and Div_{Q_n} buffer outputs were used to connect the PLL divider, while outputs Div_{L_p} and Div_{L_n} were left unconnected. Both divider buffers were however active, thereby improving the phase balance of the QVCO. In the I/Q phase error detector circuit [7, 8], all four outputs were used to connect the detector.

To minimize capacitive losses to the substrate, the inductors are implemented in the top Cu layer. The octagonal inductors are sized with an inner diameter of 50 μm and a trace width of 11 μm . Their differential inductance equals 120 pH with a Q value of 18 at 28 GHz [7, 8]. The transformer used for extraction of the 56 GHz second harmonic has primary side input nodes In_{56_p} and In_{56_n} connected to the emitters of the QVCO core devices. The secondary side output nodes, Out_{56_p} and Out_{56_n} , are connected to the LO buffer in Fig. 4(b). The transformer has an inner diameter of 31 μm and a trace width of 7.4 μm . Due to the layout of the active part of the QVCO and its varactors, series wires with a length of 100 μm are required to connect the 56 GHz transformer.

In Fig. 10, a Momentum view of the two-turn 28 GHz mixer load inductors, the 56 GHz LO buffer output transformer and the 56 GHz mixer output transformer connected to the PA input is shown. The 28 GHz mixer outputs are connected to the nodes $Mix_{28_I_p}$, $Mix_{28_I_n}$, $Mix_{28_Q_p}$ and $Mix_{28_Q_n}$, respectively. To save die area and increase the inductance in order to resonate with the output capacitance of the 28 GHz mixer, the load inductors have been implemented with two turns. The inductor has an inner diameter of 53 μm and a trace width of 3.9 μm . The transconductance stage of the 56 GHz mixer, given in Fig. 5, is connected to the output nodes of the 28 GHz mixer load inductors. The interconnect wires from the load

Fig. 9 QVCO inductor plus buffer routing and 56 GHz transformer layout

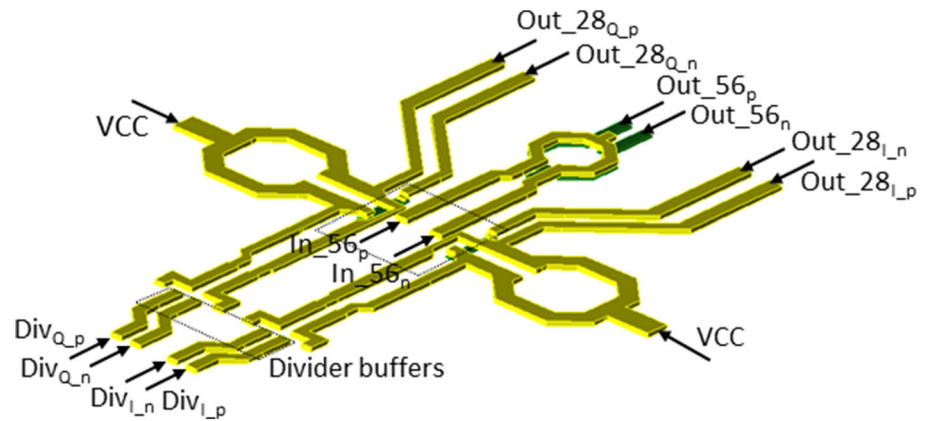
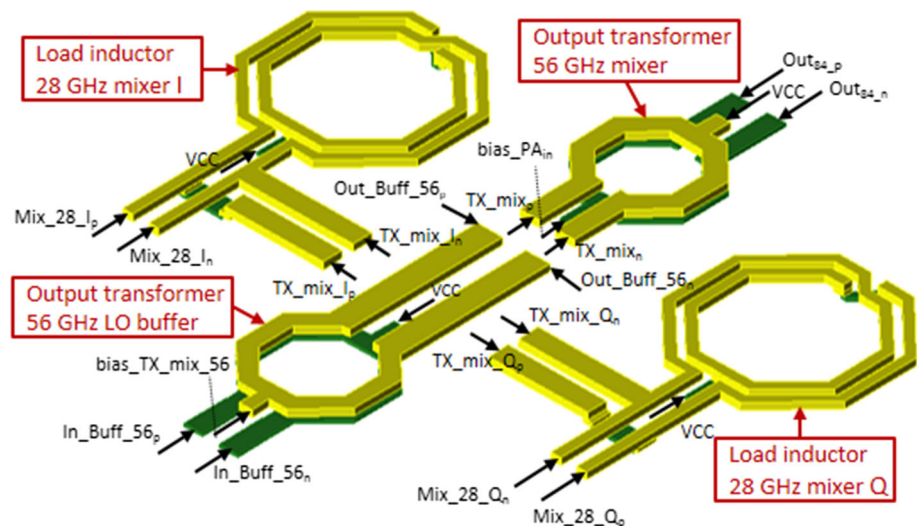


Fig. 10 Transformer for 56 GHz LO buffer, 28 GHz mixer load inductors and 56 GHz mixer output transformer



inductors to the 56 GHz mixer have been made wide to decrease the series inductance.

The 56 GHz LO buffer, shown in Fig. 4(b), has its collectors connected to the nodes $In_Buff_56_p$ and $In_Buff_56_n$ of its output transformer. The transformer was designed with an inner diameter of 35 μm and a trace width of 6.5 μm . The output nodes on the secondary side, $Out_Buff_56_p$ and $Out_Buff_56_n$ are connected to the bases of the 56 GHz mixer current-commutating devices, see Fig. 5. A center tap on the secondary side, node $bias_TX_mix_56$, is used for mixer base biasing. As can be realized from Fig. 10, the series inductance of the routing from the 56 GHz LO buffer output transformer to the 56 GHz mixer is significant in comparison with the inductance of the transformer itself, resulting in unwanted resonances. The wires have therefore been scaled up to the maximum allowed width of 10 μm . The collectors of the 56 GHz mixer are connected to the nodes TX_mix_p and TX_mix_n of its output transformer. The primary side is implemented in the top Cu layer, yellow color, due to design kit current density rules. The input to the first stage

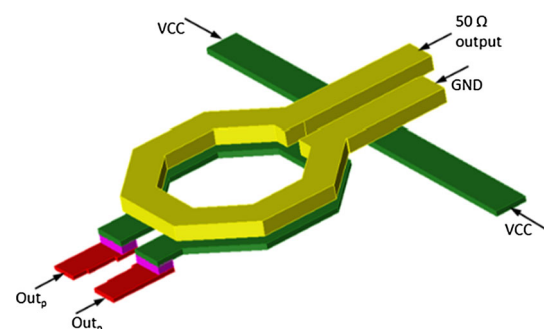


Fig. 11 Power amplifier output transformer

of the PA is connected to the nodes Out_{84_p} and Out_{84_n} , respectively. A center tap is used for PA input biasing.

For the transformers in a PA, the performance of the output transformer is the most important, since its loss has a strong impact on PA efficiency. To reduce the substrate loss, all transformers were designed in the two top Cu layers with 2.8 μm Cu4 and 1.05 μm Cu3. The output transformer, shown in Fig. 11, has an inner diameter of

24 μm and a trace width of 5.6 μm . The supply voltage of the output stage is connected through a center tap on the primary inductor. For maximum gain, and to minimize the loss, the transformer inductance and the output capacitance of the output stage must be in resonance at the transmit frequency of 84 GHz. For each of the four transformers in the presented PA design, the loss is in the range of 1 dB.

For a certain current handling capability of the output devices, a minimum device size is required, thereby determining the maximum transformer inductance. Further, since the diameter of the transformer in our case is in the same size range as the width of the output device, it is important to model the transformer including the Cu2 connection to the active device. For Momentum modelling, the trace length to the center of the active device has therefore been added to the transformer structure.

4.2 Transformer/inductor lumped model

S-parameter models of the transformers and inductors were used for simulations using SpectreRF PSS with the harmonic balance option. However, time domain simulations with S-parameter models, such as transient simulations, can give inaccurate results due to convergence difficulties. The reason is that the Momentum simulator creates models in the frequency domain that do not work well in the time domain. Transient simulations were, however, required to evaluate the EVM performance of the transmitter with digitally modulated input signals. Therefore, simplified lumped equivalent models, as shown in Fig. 12, were created for all transformers and inductors of the transmitter.

The model uses five fitting parameters: the primary and secondary side inductance, L , the series resistance of the inductance, R_s , the parasitic capacitance to ground of the primary side, C_{in} , the parasitic capacitance to ground of the primary side, C_{out} , and the coupling coefficient k . To keep

the model simple, it does not include any interwinding capacitance. When applicable, the model has been extended with series inductances due to routing on the primary and secondary side. Even with a limited number of lumped elements as in Fig. 12, it is possible to achieve a good match regarding transformer impedances and insertion loss at the transformer operating frequencies.

4.3 Transmitter layout

The layout of the transmitter is shown in Fig. 13. The total size of the design equals 890 $\mu\text{m} \times 450 \mu\text{m}$, of which more than 30% can be used for additional on-chip decoupling. In total there are 10 inductors and transformers, which dominate the occupied die area. The supply voltage is connected to the top metal layer (yellow color), while the ground is connected to the bottom layer (blue color). High Q metal-oxide-metal (MOM) decoupling capacitors between supply and ground have been created by connecting the two top metal layers to the supply and the two bottom metal layers to ground.

The QVCO is located to the left, followed by the transformer to extract the 56 GHz LO signal. The design has been made symmetrical, i.e. the two 28 GHz mixers are located above and below the 56 GHz LO buffer, while the 56 GHz mixer is placed in the center. A symmetrical layout is highly important, since differences in wire length can otherwise result in impairments of the transmitted signal. Due to the size of the transformers, the distance is quite long between the QVCO core and the 56 GHz mixer, thereby requiring LO signal buffering. The baseband signals are connected to the top and bottom side of the I and Q 28 GHz mixers, respectively. The three-stage PA is located to the right of the 56 GHz mixer.

5 Transmitter and building blocks circuit simulation

5.1 Power amplifier simulation results

The performance of the three stage PA, including the transformer between the 56 GHz mixer and the PA, was simulated with the output loaded with a pad in the top metal layer and a 50 Ω resistor. This emulates a measurement setup where the PA output is connected to ground-signal-ground (GSG) pads. The input terminals, TX_p and TX_n were for optimum input matching driven by a 95 Ω differential port in parallel with a 35fF capacitor. The small signal S-parameters are given in Fig. 14. At 84 GHz, S_{21} equals 20.6 dB with a -3 dB bandwidth of 7.2 GHz. The output matching, given by S_{22} equals -5.7 dB at 84 GHz. A wide input match is important for the ability of

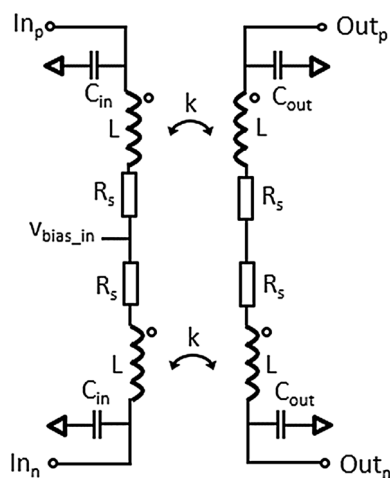


Fig. 12 Lumped model transformer equivalent

Fig. 13 Complete E-band transmitter layout

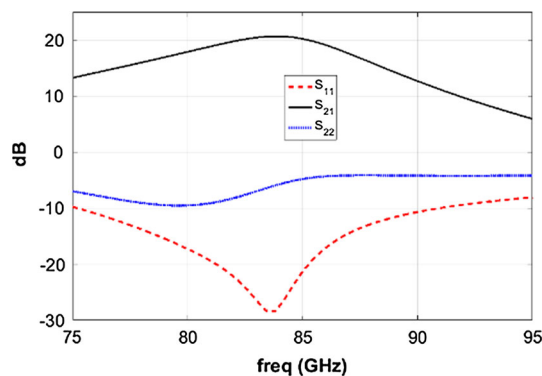
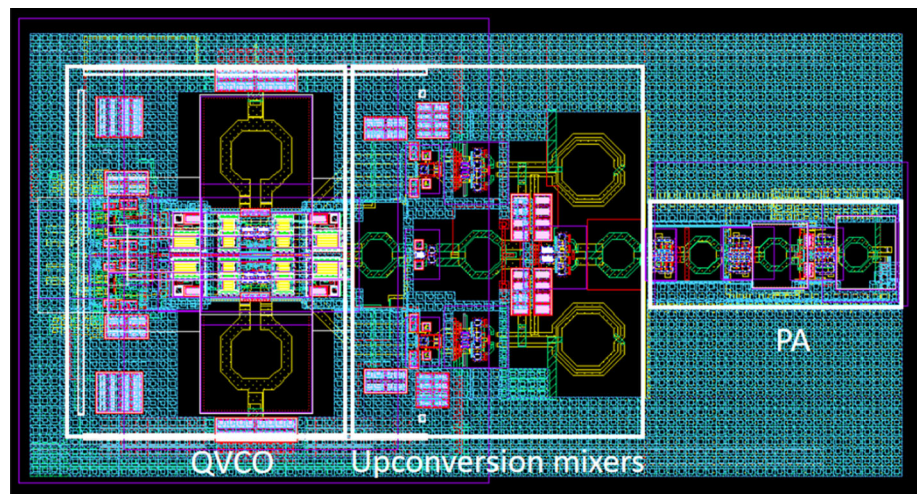


Fig. 14 Power amplifier s-parameters

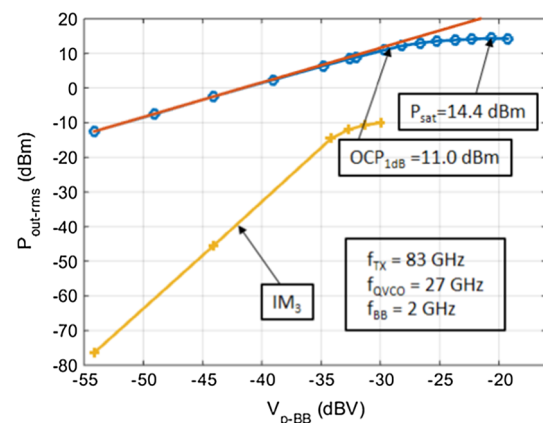


Fig. 16 Output power of the complete transmitter at 83 GHz versus baseband input level

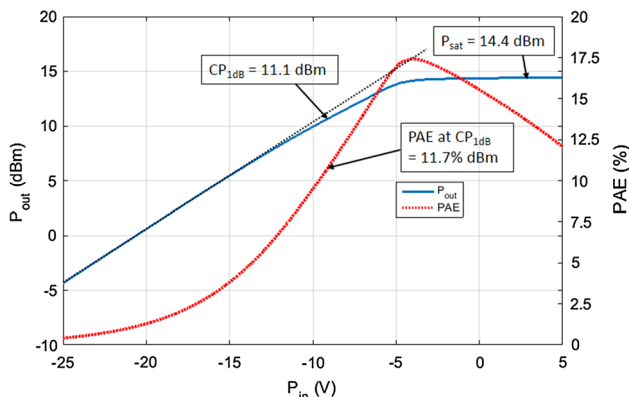


Fig. 15 Power amplifier large signal performance

the 56 GHz mixer to drive the PA into compression. The first stage of the PA has thus been designed so that $S_{11} < -10$ dB for a frequency range of 16 GHz.

The large signal simulation results are given in Fig. 15, showing output power and power added efficiency (PAE) versus input power. The PA achieves a saturated output power, P_{sat-PA} , of 14.4 dBm, while the 1 dB output

compression point, OCP_{PA-1dB} , is 11.1 dBm. When transmitting with M-QAM modulated input signals a high compression point is advantageous, since low EVM is required. The peak PAE equals 17.4%, while it is 11.7% at CP_{1dB} .

5.2 Transmitter simulation results with non-modulated signals

The periodic steady-state (PSS) harmonic balance analysis in SpectreRF was used to simulate the transmitter performance with non-modulated signals. Due to simulator convergence difficulties, it was not possible to use a device level representation of the QVCO. In these simulations, the QVCO, was therefore replaced with ideal time-delayed sinusoidal voltage sources. With a baseband frequency, f_{BB} , at 1 GHz, the frequency at the PA output, f_{TX} , is at 84 GHz for a QVCO frequency, f_{QVCO} , of 27.7 GHz. In the PSS analysis both the LO signals and the baseband signals are defined as large signals. The I and Q baseband signals were

phase shifted by 90° . The inductors and transformers of the upconverter and PA were represented with S-parameter models. The output power at 83 GHz versus baseband differential peak voltage, V_{p-BB} , is shown in Fig. 16. In order to decrease the simulation time and the number of harmonics, and to achieve 83 GHz transmit frequency, the baseband frequency was set to 2 GHz. Using the harmonic balance simulator, the QVCO frequency must also be at a harmonic of the PSS fundamental frequency. The third order distortion was simulated with a PAC-signal at 2.1 GHz.

As seen from Fig. 16, the transmitter can deliver a saturated output power, P_{sat-TX} of 14.4 dBm with an output compression point OCP_{TX-1dB} equal to 11 dBm. In Fig. 17, P_{sat-TX} and OCP_{TX-1dB} is simulated versus f_{TX} for f_{BB} equal to either 1 GHz or 2 GHz depending on the desired transmit frequency. Within the 81–86 GHz band, P_{sat-TX} varies between 14.2 and 14.5 dBm, while OCP_{TX-1dB} varies between 11.0 and 13.4 dBm.

6 System simulation

6.1 Error vector magnitude (EVM) in Transmitters

For a high data-rate wireless link using QAM modulation, the transmitter linearity, LO phase noise and I/Q phase imbalance are highly important [16–20], since they impact the achievable BER. During the design of a MM-wave transmitter it is therefore of great value if the expected BER due to transmitter imperfections can be estimated. However, both measuring and simulating the BER is significantly more complicated than using the EVM, from which the BER can then be estimated. In the presented work, the EVM is calculated based on demodulated I and Q signals from transient simulations. In (1) [22, 36] the bit

error rate, P_b , is related to the signal to noise ratio, E_s/N_0 , with Q being the Gaussian co-error function [36]. L is equal to the number of levels in each dimension in the constellation diagram and M is the order of the quadrature amplitude modulation, i.e. for 16 QAM, M is equal to 16 and L is equal to 4.

$$P_b \approx \frac{2(1 - \frac{1}{L})}{\log_2 L} Q \left[\sqrt{\frac{3 \log_2 L}{L^2 - 1}} \frac{2E_s}{N_0 \log_2 M} \right] \quad (1)$$

For large symbol streams, the EVM is related to the signal to noise ratio as given by (2)

$$EVM_{RMS} \approx \left[\frac{1}{SNR} \right]^{\frac{1}{2}} = \left[\frac{N_0}{E_s} \right]^{\frac{1}{2}} \quad (2)$$

Using (1) and (2), the bit error rate, P_b , can be directly related to the EVM_{RMS} as in (3) [22],

$$P_b \approx \frac{2(1 - \frac{1}{L})}{\log_2 L} Q \left[\sqrt{\frac{3 \log_2 L}{L^2 - 1}} \frac{2}{EVM_{RMS}^2 \log_2 M} \right] \quad (3)$$

In the constellation diagram for 16 QAM, 4 bits are mapped to each transmitted symbol, see Fig. 18(a).

The definition of the Error Vector Magnitude (EVM) is illustrated in Fig. 18(b) [17–20], showing the difference between an ideal transmitted constellation point and the actual transmitted point. The rms error vector magnitude, EVM_{rms} , is defined in (4) [21], as the normalized root mean square value of the errors of a large number (N) of constellation points.

$$EVM_{RMS} = \left[\frac{\frac{1}{N} \sum_{r=1}^N |S_{ideal,r} - S_{meas,r}|^2}{\frac{1}{N} \sum_{r=1}^N |S_{ideal,r}|^2} \right]^{0.5} \quad (4)$$

$$EVM_{dB RMS} = 20 \log EVM_{RMS} \quad (5)$$

In [22], the bit error rate is plotted versus EVM, using (3), for different modulation schemes. The results correspond well with Monte Carlo simulations. As expected, higher modulation order results in more stringent EVM requirements for a certain bit error rate. For 16 QAM, a BER of $3e-6$ is achieved for 20 dB EVM_{RMS} . In linear scale, this corresponds to 10% EVM_{RMS} . With increasing EVM_{RMS} , the BER quickly degrades, e.g. 18% EVM_{RMS} , gives a BER of $3e-3$. Early E-band links typically used simple modulation schemes, like BPSK. According to [22], BPSK is much more robust, but the bandwidth efficiency is heavily compromised. For long-distance links, however, lower order modulation schemes are often used to increase the communication robustness. Typically E-band commercial systems use adaptive modulation techniques that changes the modulation type depending on the quality of the radio channel. There is an optimal modulation scheme that maximizes the user data throughput. With too

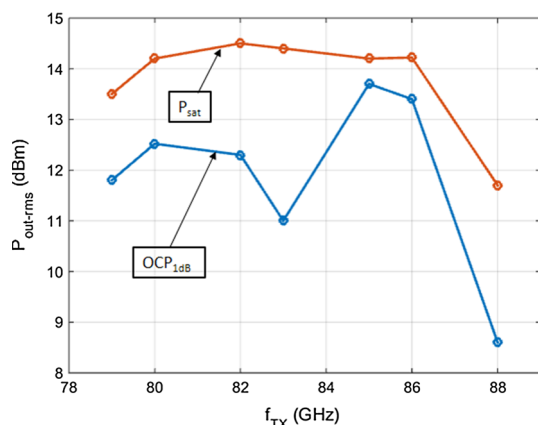
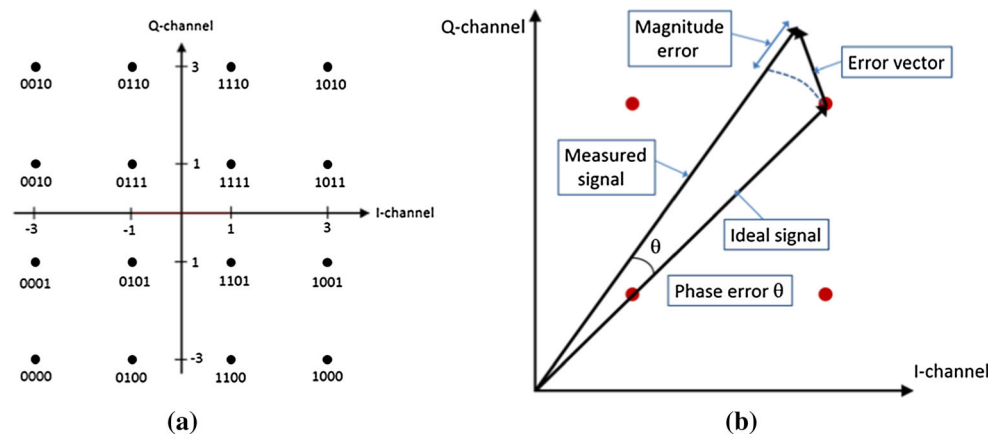


Fig. 17 Complete transmitter $P_{sat-TX-1dB}$ and OCP_{TX-1dB} versus transmit frequency

Fig. 18 Constellation diagram for 16 QAM (a) and definition of EVM (b)



high a modulation order, more bits are required for error-correcting coding, thereby lowering the user data throughput. On the other hand, with too low a modulation order, less coding is required but the data throughput is unnecessarily low. One source of EVM is the phase noise of the local oscillator. The 28 GHz QVCO used in this work [7–9], has a measured phase noise of -100 dBc/Hz at 1 MHz offset [8]. A second source of EVM is the I/Q phase imbalance [17–20]. A third source is large signal distortion [19, 20]. The nonlinearity of especially the PA has a large impact on EVM, since it operates with the largest signals in the transmit chain. The PA exhibits two types of distortion that impact the EVM. AM to AM compression and AM to PM conversion [19]. The first mechanism compresses the magnitude of the sum of the I and Q signals [19]. Especially signals at the corners of the constellation, which have the highest magnitude, are affected. To reduce this effect the input power to the PA must be reduced so that the level is well below the PA compression point at all times. The second effect manifests itself as a phase shift in the I/Q constellation diagram that depends on the input amplitude [19]. The symbols with higher amplitude, i.e. the outer ones, will then be rotated more than the inner symbols. Using PA power back-off, also these effects of insufficient linearity can be mitigated, however, at the cost of reduced PA efficiency. The PA normally has the highest power consumption of the blocks in the transmitter, and it is therefore desirable to operate it as close as possible to its OCP_{1dB} where the PAE is the highest. Digital predistortion (DPD) of the baseband signal [19] can also be used to improve the EVM. However, linearity improvements using e.g. predistortion are easier to implement if the transmitter itself has a low EVM. Another source of imperfection, though not investigated in this work, is carrier leakage in the 28 GHz I/Q mixer [22], resulting in a DC-shift of the constellation diagram. Carrier leakage minimization typically requires digital tuning to counteract circuit imbalances.

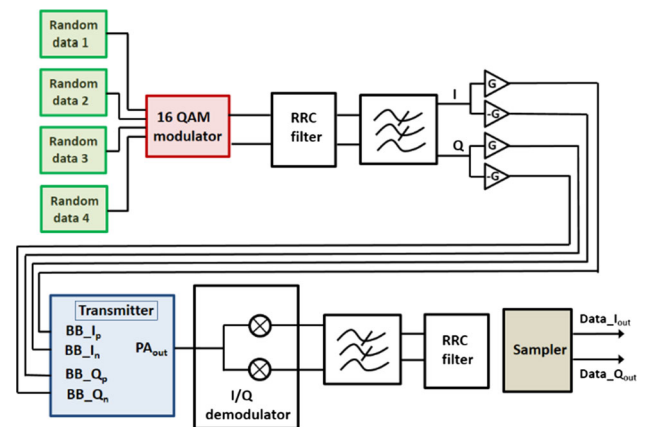


Fig. 19 Simulation setup for generating digitally modulated input signals

6.2 System simulation setup

The EVM has been simulated for a 1 GHz 16 QAM signal. Four random data streams, generated in a module from the Cadence library *ahdlLib*, at a data rate f_{BB} equal to 1 GHz, were supplied to a Verilog-A 16 QAM generator creating I and Q signals, as outlined in Fig. 19. The data is first filtered in an RRC filter [37]. The purpose of the RRC filter is to reduce out of channel spectral emissions with a limited impact on the peak-to-average power ratio (PAPR) [37, 38] and intersymbol interference (ISI) [38]. In this work an RRC filter implemented in Verilog-A with a roll off factor equal to 0.22, from the Cadence library *rfLib*, has been used. Before upconversion, the digitally modulated baseband signals need to be further low pass filtered to avoid excess leakage of signal images into neighboring channels. This is accomplished by a Verilog-A second order Butterworth low pass filter from the *rfLib*. After single-ended to differential signal conversion, the modulated signal is supplied to the transmitter baseband input.

At the detector side, the PA output signal is supplied to a Verilog-A I/Q demodulator from *rfLib*, clocked at a

frequency f_{demod} equal to 84 GHz. After filtering in an analog low pass filter, followed by the RRC filter, the I and Q outputs are sampled at a rate equal to f_{BB} . A flow chart for the EVM calculation is given in Fig. 20. The simulated I and Q data, $Data_I_{out}$ and $Data_Q_{out}$ in Fig. 20, cannot be directly compared with the transmitted data, $Data_I_{sent}$ and $Data_Q_{sent}$, since it is rotated in phase and has an amplitude that depends on the transmitter gain. Therefore, the I/Q data must first be normalized.

An initial gain calculation is based on the amplitude ratios, G_{norm} , between the four transmitted and detected inner points of the constellation diagram. Only the four inner points are used for the initial gain calculation, since compared to the 12 outer points, these are less affected by transmitter compression. The detected data is first normalized with G_{norm} . The EVM_{rms} , calculated using (4), has a minimum for a certain fine tuning gain, G_{fine} , controlled in a gain sweep. The gain optimization is repeated for each phase position controlled by the phase sweep. The gain and phase settings resulting in minimum EVM are then used in the final calculation.

6.3 Transmitter EVM simulation results

The EVM of the complete transmitter has been simulated with a 16 QAM 1 GHz signal. The EVM dependency on average PA output power, $P_{out-RMS}$, QVCO phase noise, and QVCO I/Q phase imbalance have been investigated. In Fig. 21, the EVM dependency on $P_{out-RMS}$ is shown for a setup with no I/Q phase error and with noiseless devices. At low enough output power, the transmitter is linear and thus does not distort the constellation diagram. For average output powers above 0 dBm, the EVM increases rapidly though. With a PAR of 2.55 dB for 16 QAM, the amplitudes of the 4 outer symbols of the constellation diagram will be close to the OCF_{dB} for an output power of 7.5 dBm, giving 6.4% EVM. For $P_{out-RMS}$ back-off to 5 dBm the EVM is improved to 3.5%. The EVM is dominated by the compression of the PA.

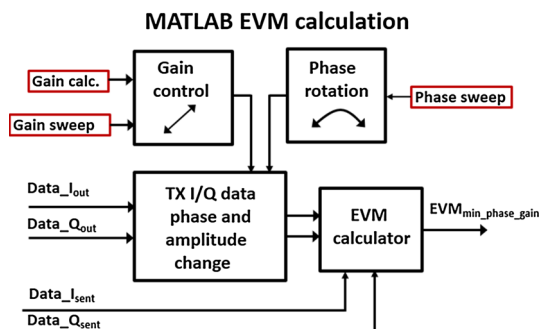


Fig. 20 MATLAB blocks for EVM calculation

The simulated relationship between EVM and QVCO phase noise level at 1 MHz offset is shown in Fig. 22. The simulation was performed for a small PA output signal and without I/Q phase error. As can be seen, the EVM is equal to 1.8% even for a phase noise level of -120 dBc/Hz. This is due to that during the transient noise analysis, all noise sources in the devices are turned on, not only in the QVCO. At a measured phase noise level of -100 dBc/Hz [8], the EVM equals 3.6%, i.e. the QVCO phase noise adds 1.8% to the EVM. Further decreasing the phase noise would increase the QVCO power consumption significantly.

Inside the PLL bandwidth the phase noise will be reduced, thereby improving the EVM performance. The performed simulation thus provides a safe estimate of allowed QVCO phase noise. In [9], the PLL measured phase at 1 MHz offset equals -107 dBc/Hz. In Fig. 23, the EVM is simulated versus QVCO I/Q phase error. The simulations were performed for a low PA output level and

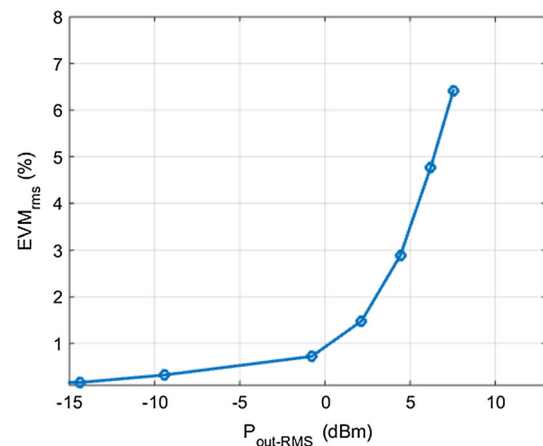


Fig. 21 EVM versus $P_{out-RMS}$ without I/Q phase error and device noise

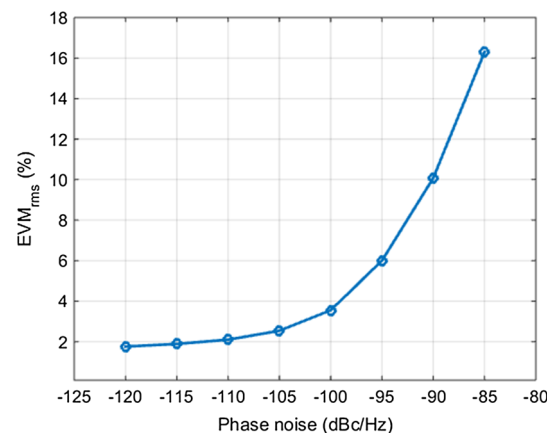


Fig. 22 EVM versus QVCO phase noise at 1 MHz offset at low output power and no I/Q phase error

with the noise sources turned off. As can be seen even an I/Q phase error as small as 3° results in an EVM of 2.8%, thereby stressing the need for I/Q phase error calibration.

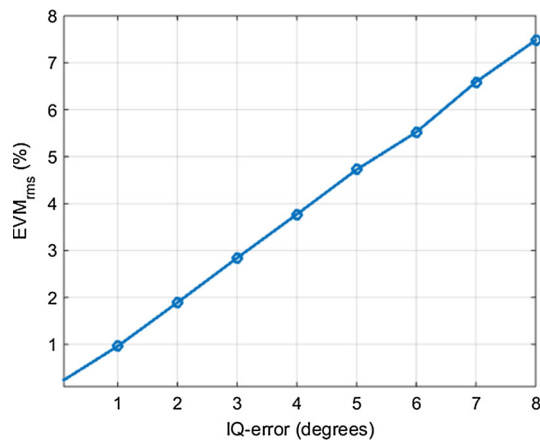


Fig. 23 EVM versus QVCO I/Q phase error at low output power with noiseless devices

One way of implementing the I/Q phase calibration is shown in Fig. 2(a) [7, 8].

The effects on the 16 QAM constellation diagram of the three separately investigated transmitter impairments, together with the combined effects, are shown in Fig. 24. The effect of compression is shown for $P_{\text{out-RMS}}$ equal to 7.5 dBm, see Fig. 24(a). The effect of a QVCO phase noise level of -90 dBc/Hz is shown in Fig. 24(b), while the effect of an I/Q phase error equal to 6° is given in Fig. 24(c). The combined effect of all three impairments in Fig. 24(d), with $P_{\text{out-RMS}}$ equal to 7.5 dBm, PN at 1 MHz offset equal to -100 dBc/Hz, and an I/Q phase error equal to 1° is shown in Fig. 24(d), giving an EVM of 7.2%. An I/Q phase error of 1° is the accuracy that can be achieved using the phase error detector and tuner presented in [7] and [8]. In this case the EVM is dominated by the compression effect, giving 6.4% EVM, see Fig. 21.

As can be seen in Fig. 24(a), too high an output power causes gain compression of the outer points in the constellation diagram. The QVCO phase noise causes a

Fig. 24 Impact on 16 QAM constellation diagrams from investigated transmitter impairments: compression (a) phase noise (b) I/Q phase error (c) and combined effects (d)

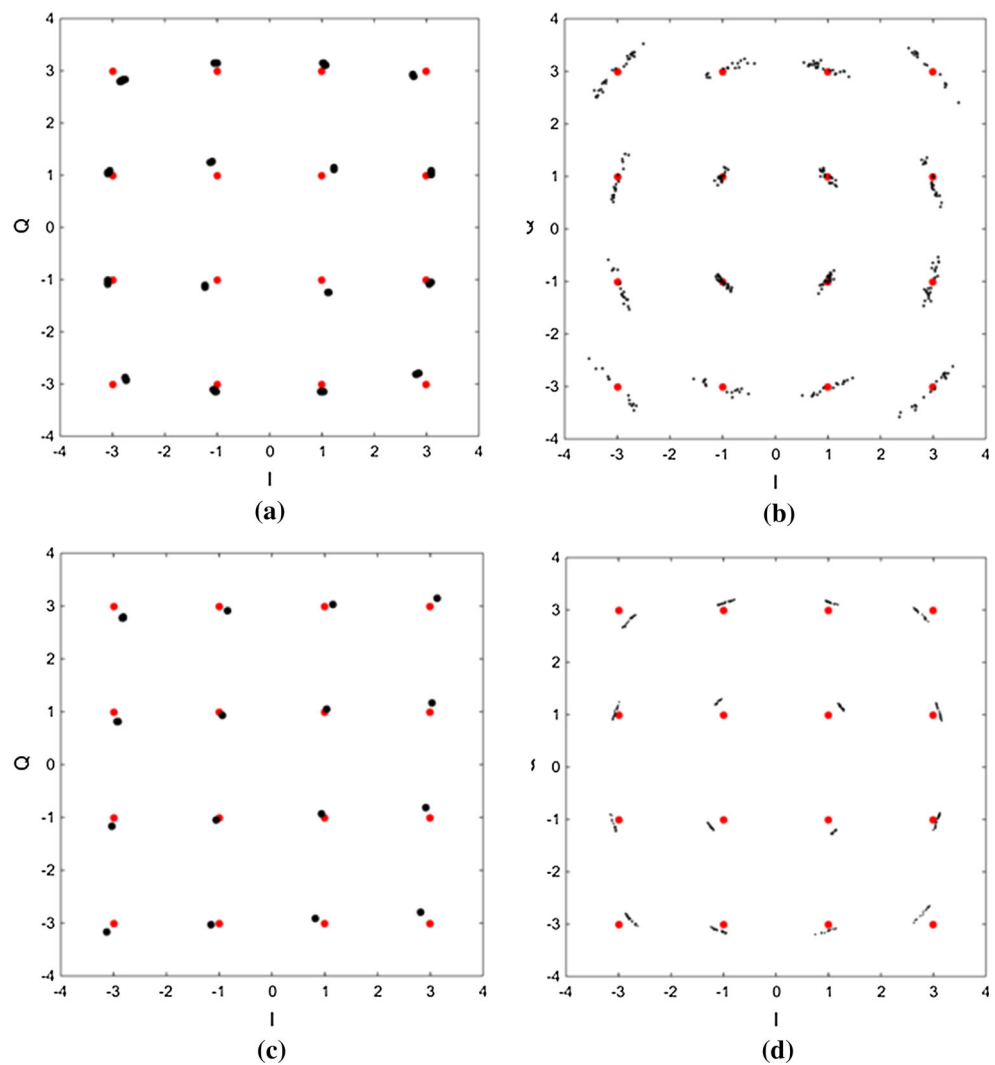


Table 1 Transmitter performance summary

Parameter	Value	Unit	Note
Supply voltage	1.5	V	Common supply for complete TX including PA
P_{DC} complete TX	196	mW	PA output power well below OCP_{1dB}
P_{DC} PA only	87	mW	PA output power well below OCP_{1dB}
QVCO: PN @ 1 MHz offset	−100	dBc/Hz	Measured value [8]
QVCO frequency range	26.0–31.0	GHz	Measured values [8]
PAE PA only	11.7	%	PAE at OCP_{1dB}
P_{sat} complete TX	14.2	dBm	Min P_{sat} between 81 and 86 GHz
OCP_{1dB} complete TX	11	dBm	Min CP_{out} between 81 and 86 GHz
EVM for $P_{out_RMS} = 7.5$ dBm	7.2	%	1 GHz 16 QAM, QVCO PN = −100 dBc/Hz @ 1 MHz offset, I/Q phase error = 1, including noise effects

rotational random shift of the constellation points, while the I/Q phase error results in a skewed constellation. The simulated transmitter performance is summarized in Table 1.

7 Conclusions

This paper presents system simulation results for an 81–86 GHz E-band transmitter based on a 28 GHz QVCO. Up conversion to 84 GHz carrier frequency is performed with mixing of the 56 GHz differential second harmonic present at the emitters of the QVCO core cross coupled transistors. Basing the transmitter on a 28 GHz QVCO instead of an 84 GHz QVCO is advantageous, since the I/Q phase error will be significantly reduced for a lower frequency QVCO due to less impact of mismatch in capacitive and inductive parasitics. System simulations, investigating effects of compression, phase noise and I/Q phase imbalance have demonstrated the transmitter performance for a 1 GHz 16 QAM signal. The impact of phase noise on the EVM has been investigated by using a Verilog-A equivalent model of the QVCO with controllable phase noise. The QVCO has a nominal phase noise of −100 dBc/Hz at 1 MHz. For the system simulations, lumped equivalent models were used for all transformers and inductors in the design. For the circuit simulations with continuous baseband signals, S-parameter transformer models were instead utilized. In the E-band at 81–86 GHz, the saturated PA output power exceeds 14.4 dBm with an output compression point of 11 dBm. With 16 QAM modulation the transmitter achieves an EVM_{rms} of 7.2% at an average output power of 7.5 dBm. This corresponds to a BER of less than $1e-6$ [22]. Transmission with an increased EVM is possible, but reduces the user data throughput due to an increased number of bits used for coding. Below the OCP_{1dB} , the complete transmitter

including the PA consumes 131 mA from a common 1.5 V supply.

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